**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

Zoran Krivokapic	:	Group Art Unit: 2812
Application No.: 10/601,401	:	Examiner: Stanetta D. Isaac
Filed: June 23, 2003	:	

Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Sir:

Attached hereto is a completed Form PTO-1449 listing patents, publications, or other information which the applicant believes may be material to the examination of this application, with copies of each such item enclosed herewith. It is requested that the cited patents be made of record in the examination of this application. I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than 3 months prior to the filing of this statement. The commissioner is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 50-2173.

Respectfully submitted,

Dated: 31 March 2005

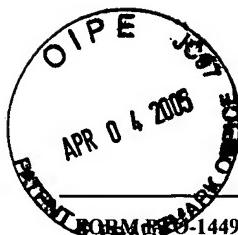
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CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this document (and any as referred to as being attached or enclosed) is being deposited with sufficient postage as first class mail with the United States Postal Service on March 31, 2005 and addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Colleen T. Bonner
 Colleen T. Bonner



Sheet 1 of 1

<div style="text-align: right; margin-bottom: 10px;">  U.S. DEPARTMENT OF COMMERCE </div> <div style="text-align: center; margin-bottom: 10px;"> PATENT AND TRADEMARK OFFICE </div> <div style="text-align: center; font-weight: bold;"> INFORMATION DISCLOSURE STATEMENT BY APPLICANT </div> <p>(Use several sheets if necessary)</p>	ATTY. DOCKET NO. <i>H1938</i>	SERIAL NO. <i>10/601,401</i>
	APPLICANT <i>Zoran Krivokapic</i>	
	FILING DATE <i>June 23, 2003</i>	GROUP <i>2812</i>

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	2001/0036731	11/01/01	Muller, et al.			
	2002/0003256	01/10/02	Maegawa			
	2003/0025126	02/06/03	Hsu			
	2003/0057486	03/27/03	Gambino, et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	2004/044992	05/27/04	WO			

OTHER DOCUMENTS (Including Author, Title, Date Pertinent Pages, Etc.)

	K. Ota, K. Sugihara, H. Sayama, T. Uchida, H. Oda, T. Eimori, H. Morimoto and Y. Inoue, Novel Locally Strained Channel Technique for High Performance 55nm CMOS, IEDM Technical Digest, December 8, 2002, pp. 27-30.
	A. Shimizu, K. Hachimine, N. Ohki, H. Ohta, M. Koguchi, Y. Nonaka, H. Sato, and F. Ootsuka, Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement, IEDM Technical Digest, December 2, 2001, pp. 433-436.

EXAMINER _____ **DATE
CONSIDERED** _____

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Form PTO-1449)